REG10J0028-0100

Renesas Starter Kit for SH7086

User's Manual

RENESAS SINGLE-CHIP MICROCOMPUTER
SuperH™ RISC engine

Rev.1.00
Revision date：13.MAR.2007

Renesas Technology Europe Ltd.
www.renesas.com

Table of Contents

Chapter 1. Preface

Cautions

This document may be, wholly or partially, subject to change without notice.

Trademarks

Copyright

Website: http://www.renesas.com/

Glossary

BRR	Baud Rate Register	ERR	Error Rate
HMON	Embedded Monitor	RSK	Renesas Starter Kit
LCD	Liquid Crystal Display	CPU	Central Processing Unit
LED	Light Emitting Diode	IVT	Interrupt Vector Table

Chapter 2. Purpose

This RSK is an evaluation tool for Renesas microcontrollers.

Features include:

- Renesas Microcontroller Programming.
- User Code Debugging.
- User Circuitry such as switches, LEDs and potentiometer(s).
- Sample Application.
- Sample peripheral device initialisation code.

The CPU board contains all the circuitry required for microcontroller operation.

This manual describes the technical details of the RSK hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

Chapter 3. Power Supply

3.1. Requirements

This CPU board operates from a 5V power supply.

A diode provides reverse polarity protection only if a current limiting power supply is used.

All CPU boards are supplied with an E8 debugger. This product is able to power the CPU board with up to 300mA. When the CPU board is connected to another system that system should supply power to the CPU board.

All CPU boards have an optional centre positive supply connector using a 2.0mm barrel power jack.

Warning

The CPU board is neither under not over voltage protected. Use a centre positive supply for this board.

3.2. Power – Up Behaviour

When the RSK is purchased the CPU board has the 'Release' or stand alone code from the example tutorial code pre-programmed into the Renesas microcontroller. On powering up the board the user LEDs will start to flash. Pressing any switch will cause the LEDs to flash at a rate controlled by the potentiometer.

Chapter 4. Board Layout

4.1. Component Layout

The following diagram shows top layer component layout of the board.

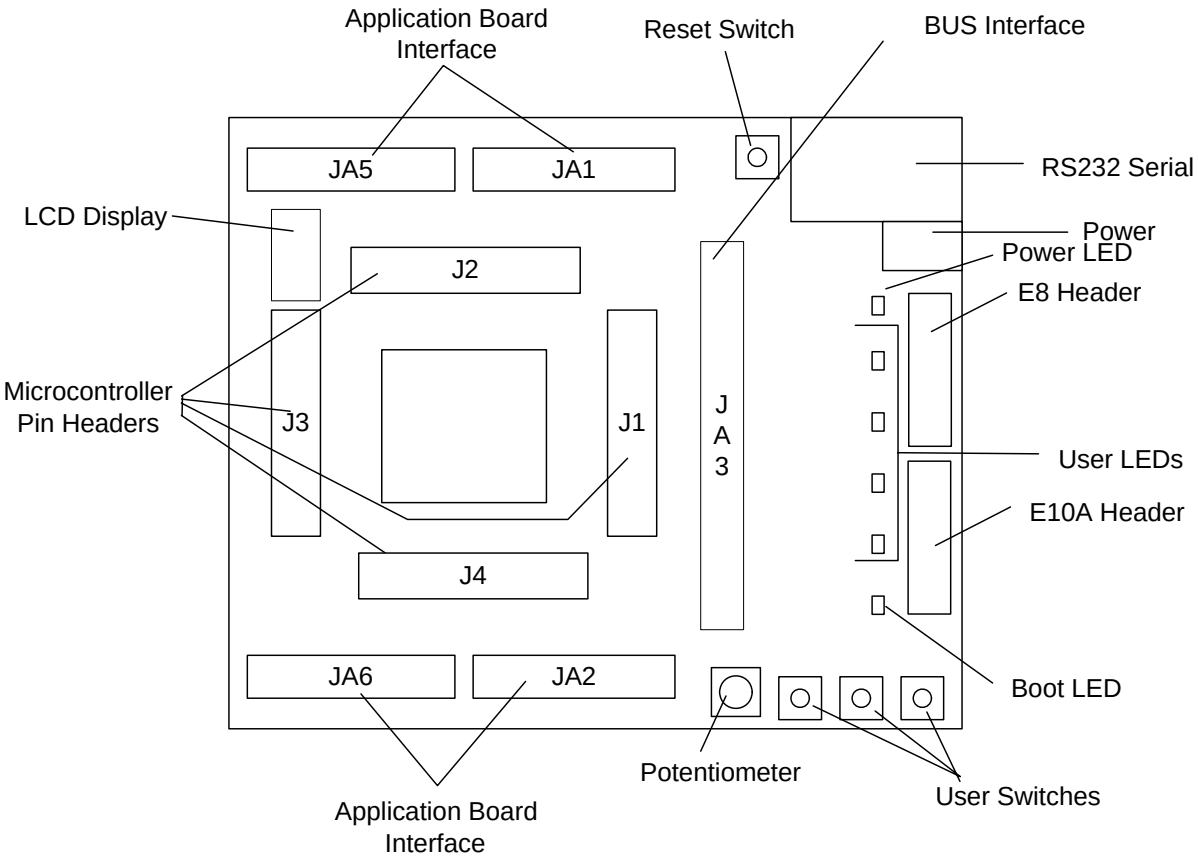


Figure 4-1: Board Layout

4.2. Board Dimensions

The following diagram gives the board dimensions and connector positions. All through hole connectors are on a common 0.1" grid for easy interfacing.

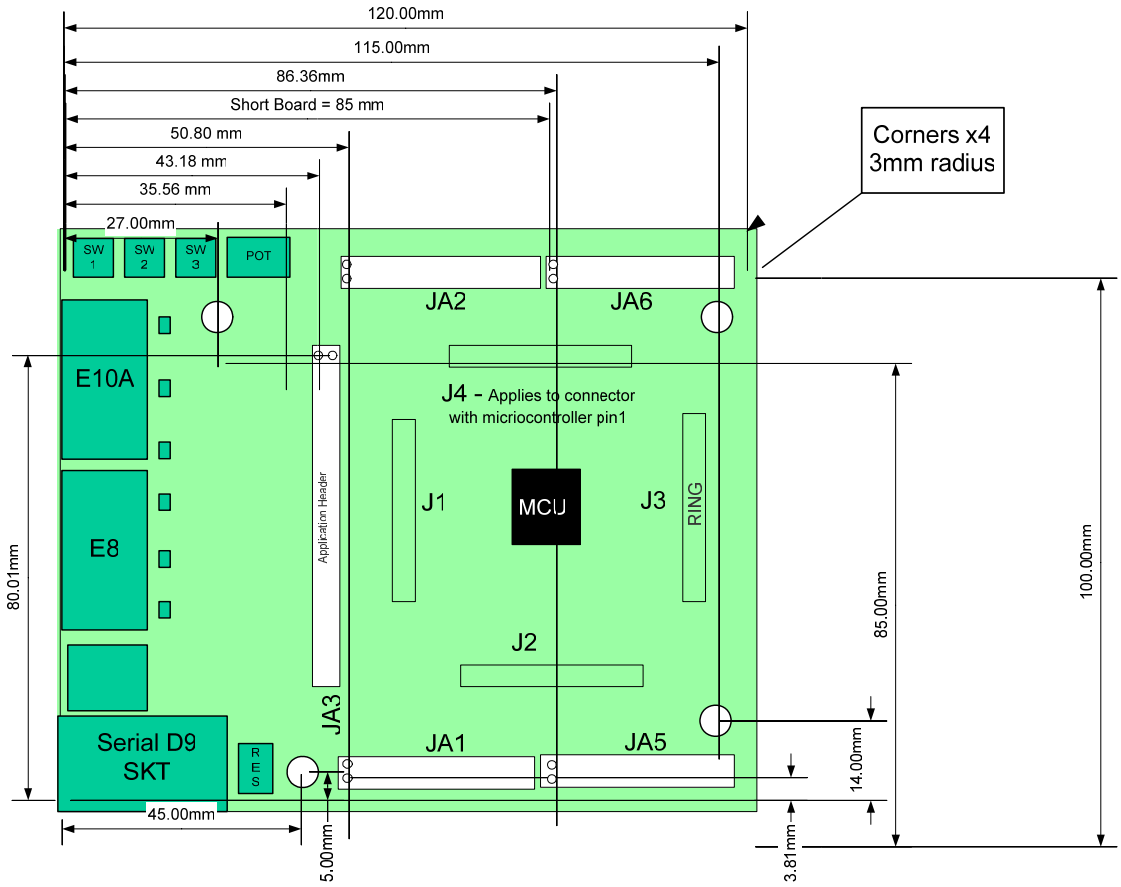


Figure 4-2 : Board Dimensions

Chapter 5. Block Diagram

Figure 5-1 shows the CPU board components and their connectivity.

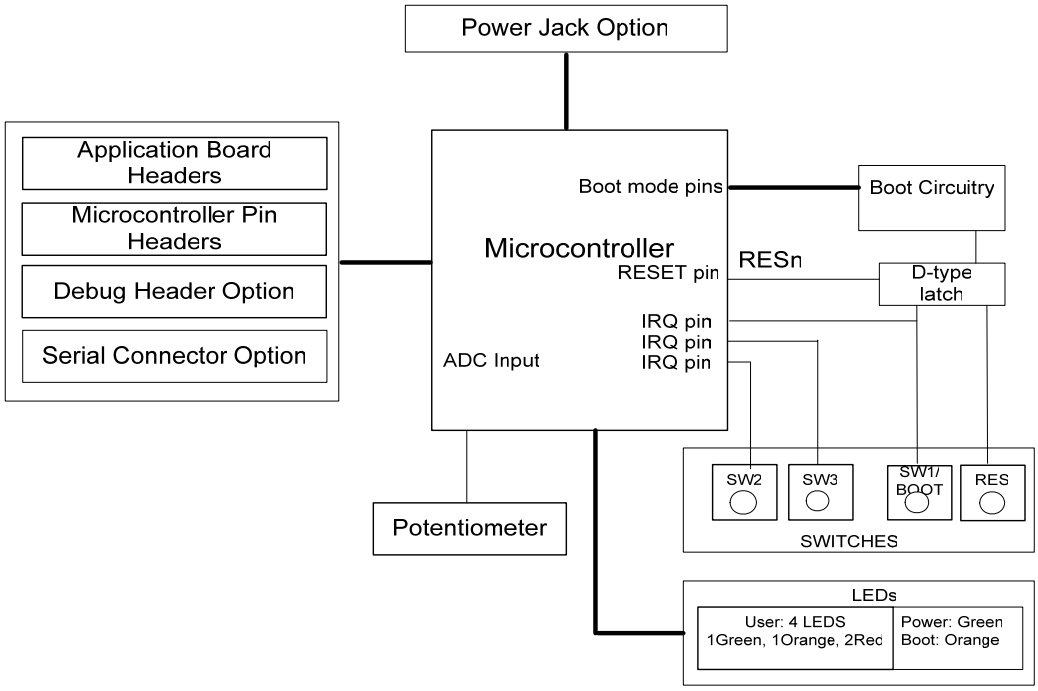


Figure 5-1: Block Diagram

Figure 5-2 shows the connections to the RSK.

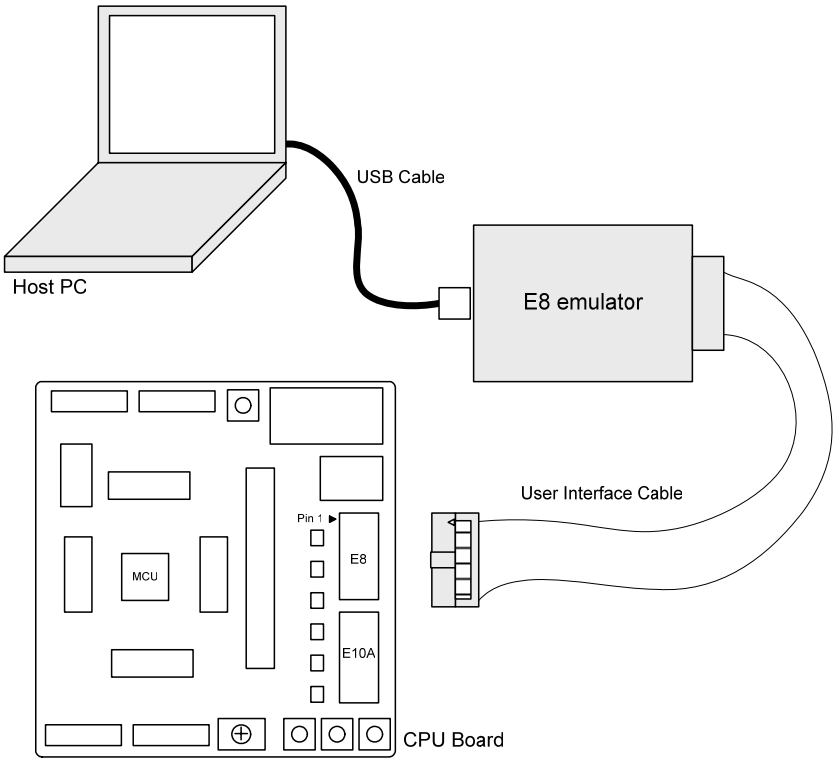


Figure 5-2 : RSK Connctions

Chapter 6. User Circuitry

6.1. Switches

There are four switches located on the CPU board. The function of each switch and its connection are shown in Table 6-1: Switch Functions

Switch	Function	Microcontroller
RES	When pressed; the CPU board microcontroller is reset.	RESn, Pin 132
SW1/BOOT*	Connects to an IRQ input for user controls. The switch is also used in conjunction with the RES switch to place the device in BOOT mode when not using the E8 debugger.	IRQ0, Pin 63 (Port A, bit 26)
SW2*	Connects to an IRQ line for user controls.	IRQ1, Pin 65 (Port A, bit 27)
SW3*	Connects to an IRQ line for user controls. Same pin functions as ADC trigger input.	IRQ7, Pin 50 (Port B, bit 9)

Table 6-1: Switch Functions

*Refer to schematic for detailed connectivity information.

6.2. LEDs

There are six LEDs on the CPU board. The green 'POWER' LED lights when the board is powered. The orange BOOT LED indicates the device is in HMON BOOT mode when lit. The four user LEDs are connected to an IO port and will light when their corresponding port pin is set low.

The LED pin references and their corresponding microcontroller port pin connections are shown in Table 6-2: LED Port

LED Reference (As shown on silkscreen)	Microcontroller Port Pin function	Microcontroller Pin Number	Polarity
LED0	Port A bit 20	38	Active Low
LED1	Port A bit 21	6	Active Low
LED2	Port A bit 22	5	Active Low
LED3	Port A bit 23	3	Active Low

Table 6-2: LED Port

6.3. Potentiometer

A single turn potentiometer is connected to pin 'AN0' of the microcontroller. This may be used to vary the input analog voltage value to this pin between AVCC and Ground.

6.4. Serial port

The microcontroller programming serial port (SCI1) is connected to the E8 connector. This serial port can optionally be connected to the RS232 transceiver by fitting option resistors and the D connector in position 'SERIAL'. The connections to be fitted are listed in Table 6-3: Serial Options Links

Description	Function	Fit for RS232	Remove for E8	Fit for Rs232	Remove for RS232
TxD1	Programming Serial Port	R43	R43	R22	R22
RxD1	Programming Serial Port	R34	R34	R20	R20

Table 6-3: Serial Options Links

The board is designed to accept a straight through RS232 cable.

6.5. LCD Module

The LCD module supplied with the RSK can be connected to the connector 'LCD' for use with the tutorial code. Any module that conforms to the pin connections and has a KS0066u compatible controller can be used. The LCD module uses a 4 bit interface to reduce the pin allocation. No contrast control is provided; this must be set on the display module.

The pin allocation and signal names used on this connector are shown in Table 6-4: LCD Module Connections

The module supplied with the CPU board only supports 5V operation.

LCD					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	Ground	-	2	5V Only	-
3	No Connection	-	4	DLCDRS	127
5	R/W (Wired to Write only)	-	6	DLCDE	126
7	No Connection	-	8	No connection	-
9	No Connection	-	10	No connection	-
11	DLCD4	43	12	DLCD5	45
13	DLCD6	46	14	DLCD7	47

Table 6-4: LCD Module Connections

6.6. Option Links

The function of the option links contained on this CPU board are listed in Table 6-5: Serial configuration links

The default configuration is indicated by BOLD text

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R20	Serial Port Configuration	**Connects programming port (Rx) to E8 connector.**	Disconnects programming port (Rx) from E8 connector.	R22, R34, R43
R22	Serial Port Configuration	**Connects programming port (Tx) to E8 connector.**	Disconnects programming port (Tx) from E8 connector.	R20, R34, R43
R31	Serial Port Configuration	Connects Alternate serial (CH2) to D connector	**Disconnects Alternate serial from D connector.**	R49, R56, R57
R33	Serial Port Configuration	Disables RS232 Serial Transceiver	**Enables RS232 Serial Transceiver**	-
R34	Serial Port Configuration	Connects programming port (Rx) to external serial connectors.	**Disconnects programming port (Rx) to external serial connectors.**	R43, R20, R22
R43	Serial Port Configuration	Connects programming port (Tx) to external connectors (not E8).	**Disconnects programming port (Tx) to external serial connectors.**	R34, R20, R22
R44	Serial Port Configuration	Routes RS232 serial port Rx to application connector (JA6).	**Disconnects RS232 serial port Rx from application connector (JA6).**	R53
R47	Serial Port Configuration	**Connects serial port RXD0 to SERIAL D-type connector.**	Disconnects serial port RXD0 from SERIAL D-type connector.	R54
R49	Serial Port Configuration	Connects Alternate serial (CH2) to D connector	**Disconnects Alternate serial from D connector.**	R31, R56, R57
R53	Serial Port Configuration	Routes RS232 serial port Tx to application connector (JA6).	**Disconnects RS232 serial port Tx from application connector (JA6).**	R44
R54	Serial Port Configuration	**Connects serial port TXD0 to SERIAL D-type connector.**	Disconnects serial port TXD0 from SERIAL D-type connector.	R47
R56	Serial Port Configuration	Connects Alternate serial (CH2) to D connector	**Disconnects Alternate serial from D connector.**	R57, R31, R49
R57	Serial Port Configuration	Connects Alternate serial (CH2) to D connector	**Disconnects Alternate serial from D connector.**	R56, R31, R49

Table 6-5: Serial configuration links

Table 6-6: Power configuration links below describes the function of the option links associated with Power configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R4	Power Source	**Board can be powered from PWR connector.**	Disconnects the supply from PWR connector.	R25, R35, R26
R25	Power Source	Connects regulated 5V voltage source to Board_VCC.	**Disconnects regulated 5V voltage source from Board_VCC.**	R4, R35, R26
R26	Power	**Connect Board_VCC to CON_5V.**	Disconnect Board_VCC from CON_5V	R4, R25, R35
R35	Power Source	**Connects regulated 3.3V voltage source to Board_VCC.**	Disconnects regulated 3.3V voltage source from Board_VCC.	R4, R25, R26
R36	Power Supply	**Connects CON_VREF to Board_VCC**	Disconnects CON_VREF from Board_VCC	R4, R25, R26
R46	Microcontroller Power Supply	**Supply power to Microcontroller.**	Fit Low ohm resistor to measure current.	-

Table 6-6: Power configuration links

Table 6-7: Analog configuration links below describes the function of the option links associated with Analog configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R40	Voltage Reference Source	Connects pin 161 to CON_VREF on JA1.	**Disconnects pin 161 from CON_VREF.**	R42
R42	Voltage Reference Source	**Board_VCC supplies voltage to AVREF (pin 161).**	Disconnects Board_VCC from pin 161.	R40
R58	Analog Voltage Source	**Links analog ground to digital ground.**	Isolates analog ground from digital ground.	R63, R64
R63	Analog Voltage Source	**Connects Board_VCC to AVCC pins (PIN 151 and 156).**	Disconnects Board_VCC from AVCC (PIN 151 and 156).	R64, R58
R64	Analog Voltage Source	Connects AVCC pins (pin 151 and 156) to CON_VREF on JA1.	**Disconnects AVCC pins (pin 151 and 156) from CON_VREF.**	R63, R58

Table 6-7: Analog configuration links

The function of the option links associated with Pin function configuration are listed in Table 6-8: Pin function configuration links

The default configuration is indicated by **BOLD** text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R23	Pin function select	**Connects PIN 175 to TDI on E10A.**	Disconnects PIN 175 from TDI.	R50
R27	Pin function select	**Connects PIN 172 to TMS on E10A header.**	Disconnects PIN 172 from TMS.	R78
R28	Pin function select	**Connects PIN 2 to ASEBRKn on E10A header.**	Disconnects PIN 2 from ASEBRKn.	R84
R29	Pin function select	**Connects PIN 176 to TDO on E10A header.**	Disconnects PIN 176 from TDO.	R81
R37	Pin function select	**Connects PIN 174 to TRSTn on E10A header.**	Disconnects PIN 174 from TRSTn.	R83
R41	Pin function select	**Connects PIN 1 to TCK on E10A header.**	Disconnects PIN 1 from TCK.	R45
R45	Pin function select	Connects PIN 1 to M2_Vp on JA5.	**Disconnects PIN 1 from M2_Vp.**	R41
R50	Pin function select	Connects PIN 175 to TXD2 on JA6.	**Disconnects PIN 175 from TXD2.**	R23
R61	Pin function select	Connects PIN 73 to WRn on JA3.	**Disconnects PIN 73 from WRn.**	R62
R62	Pin function select	**Connects PIN 73 WRLn on JA3.**	Disconnects PIN 73 from WRLn.	R61
R65	Pin function select	**Connects PIN 143 to AD_POT.**	Disconnects PIN 143 from AD_POT.	R66
R66	Pin function select	Connects PIN 143 to AN0 on JA1.	**Disconnects PIN 143 from AN0.**	R65
R68	Pin function select	**Connects PIN 140 to TMR1 on JA2.**	Disconnects PIN 140 from TMR1.	R79
R78	Pin function select	Connects PIN 172 to SCK2 on JA6.	**Disconnects PIN 172 from SCK2.**	R27
R79	Pin function select	Connects PIN 140 to SCK3 on JA6.	Disconnects PIN 140 from SCK3.	R68
R81	Pin function select	Connects PIN 176 to M2_Un on JA5.	**Disconnects PIN 176 from M2_Un.**	R29
R83	Pin function select	Connects PIN 174 to M2_Up on JA5.	**Disconnects PIN 174 from M2_Up.**	R37
R84	Pin function select	Connects PIN 2 to M2_Wp on JA5.	**Disconnects PIN 2 from M2_Wp.**	R28

Table 6-8: Pin function configuration links

Table 6-9: Clock configuration links below describes the function of the option links associated with Clock configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R74	Clock Oscillator	Connects external clock to MCU	Disconnects external clock connection to MCU	R77, R76
R75	Clock Oscillator	Parallel resistor for crystal	Not fitted	-
R76	Clock Oscillator	Connects on board clock to MCU	External Clock Source can be connected.	R74, R77
R77	Clock Oscillator	Connects external clock to MCU	Disconnects external clock connection to MCU	R74, R76

Table 6-9: Clock configuration links

6.7. Oscillator Sources

A crystal oscillator is fitted on the CPU board and used to supply the main clock input to the Renesas microcontroller. The oscillators that are fitted and alternative footprints provided on this CPU board are detailed in Table 6-10: Oscillators / Resonators

Component		
Crystal (X1)	Fitted	10MHz (HC49/4H package)

Table 6-10: Oscillators / Resonators

Warning: When replacing the default oscillator with that of another frequency, the debugging monitor will not function unless the following are corrected:

- FDT programming kernels supplied are rebuilt for the new frequency
- The supplied HMON debugging monitor is updated for baud rate register settings.

The user is responsible for code written to support operating speeds other than the default. See the HMON User Manual for details of making the appropriate modifications in the code to accommodate different operating frequencies.

6.8. Reset Circuit

The CPU Board includes a simple latch circuit that links the mode selection and reset circuit. This provides an easy method for swapping the device between HMON Boot Mode and User mode. This circuit is not required on customers' boards as it is intended for providing easy evaluation of the operating modes of the device on the RSK. Please refer to the hardware manual for more information on the requirements of the reset circuit.

The reset circuit operates by latching the state of the boot switch (SW1) on pressing the reset button. This control is subsequently used to modify a port pin state to select which code is executed.

The reset is held in the active state for a fixed period by a pair of resistors and a capacitor. Please check the reset requirements carefully to ensure the reset circuit on the user's board meets all the reset timing requirements.

Chapter 7. Modes

This CPU board supports four MCU operating modes and three on-chip flash memory programming modes. Jumpers can be used to set the appropriate modes while E8 is not in use. User Program mode (Mode 6) may be used to run and debug user code, while Boot mode may only be used to program the Renesas microcontroller with program code.

When using the E8 debugger supplied with the RSK the mode transitions between Boot mode and User Program mode are executed automatically. The CPU board provides the capability of changing between User mode and HMON Boot mode using a latch circuit. This is only to provide a simple boot control on this board when the E8 is in use with HMON.

To manually enter HMON Boot mode, press and hold the SW1/BOOT. The mode pins are held in their boot states while reset is pressed and released. Release the boot button. The BOOT LED will be illuminated to indicate that the microcontroller is in HMON boot mode. In this mode the E8 can be used to make an HMON connection in HEW.

More information on SH7086 operating modes can be found in the device hardware manual.

7.1. FDT Settings

In the following sections the tables identify the FDT settings required to connect to the board using the E8Direct debugger interface. The E8 Debugger contains the following 'pull' resistors.

E8 Pin	Resistor
A	Pull Down (100K)
B	Pull Up (100K)
C	Pull Down (100K)
D	Pull Up (100K)

Table 7-1: E8 Mode Pin Drives

7.1.1. Boot mode

The boot mode settings for this CPU board are shown in Table 7-2: Boot mode pin settings

FWE	MD1	MD0	LSI State after Reset End	FDT Settings		
				A	B	D
1	0	0	Boot Mode	0	0	1

Table 7-2: Boot mode pin settings

The following picture shows these settings made in the E8Direct configuration dialog from HEW.

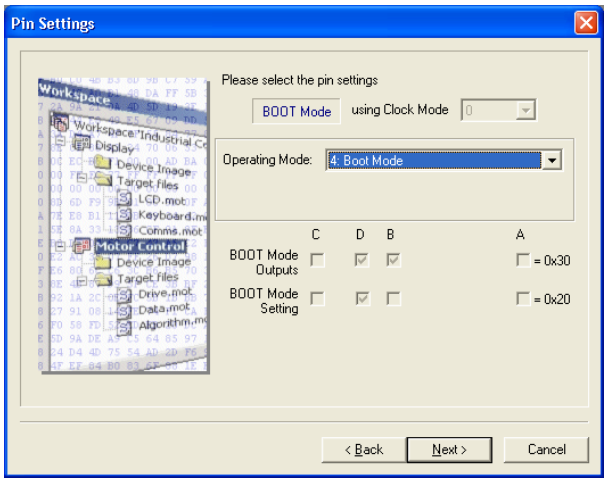


Figure 7-1: Boot mode FDT configuration

7.1.2. User Mode

For the device to enter User Mode, reset must be held active while the microcontroller mode pins are held in states specified for User Mode operation. 100K pull up and pull down resistors are used to set the pin states during reset.

FWE	MD1	MD0	LSI State after Reset End	FDT Settings		
				A	B	D
1	1	0	User Program Mode	0	1	0

Table 7-3: User Mode pin settings

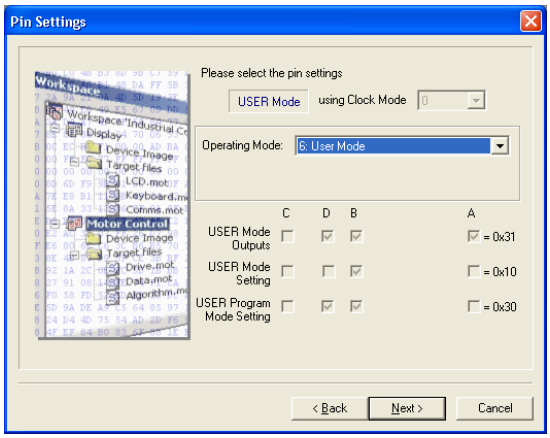


Figure 7-2: User mode FDT configuration

Chapter 8. Programming Methods

All of the Flash ROM on the device can be programmed when the device is in Boot mode. In boot mode, the boot-loader program pre-programmed into the microcontroller executes and attempts a connection with the host (for example a PC). On establishing a connection with the microcontroller, the host may then transmit program data to the microcontroller via the appropriate programming port.

The programming port for this Renesas Microcontroller and its associated pins are detailed in Table 8-1: Serial Port Boot Channel

Programming Port Table – Programming port pins and their CPU board signal names		
SCI1	TXD1, Pin 169	RXD1, Pin 167
CPU board Signal Name	PTTX	PTRX

Table 8-1: Serial Port Boot Channel

8.1. Programming with the E8

The Flash Development Toolkit (FDT) is supplied to allow programs to be loaded directly on to the board using the E8. The E8 resets the CPU invoking the User Program mode described above. This starts the FDT User Program mode programming kernel. For further information see the User program sample code and the FDT kernel code.

8.2. E10A Header

This device supports E10A debugging interface. The E10A provides additional debugging features including hardware breakpoints and hardware trace capability. (Check with the website at www.renesas.com or your distributor for a full feature list).

8.3. Serial Port Programming

This sequence is not required when debugging using the E8 supplied with the kit.

The microcontroller must enter boot mode for programming, and the programming port must be connected to a host for program download. To execute the boot transition, and allow programs to download to the microcontroller, the user must perform the following procedure:

Ensure the relevant option links are made from Table 6-3: Serial Options Links

Connect a 1:1 serial cable between the host PC and the CPU board.

Depress the BOOT switch and keep this held down.

Depress the RESET switch once, and release.

Release the BOOT switch.

The Flash Development Toolkit (FDT) is supplied to allow programs to be loaded directly on to the board using this method.

Chapter 9. Headers

9.1. Microcontroller Headers

The microcontroller pin headers and their corresponding microcontroller connections are detailed in this section. The header pins connect directly to the microcontroller pin unless otherwise stated.

* marks pins where a link to the microcontroller pin is via a fitted 0R link.

J1					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	TCK_M2Vp	1	23	VSS	23
2	ASEBRKn_M2Wp	2	24	A6	24
3	LED3	3	25	A7	25
4	M2_Vn	4	26	A8	26
5	LED2	5	27	A9	27
6	LED1	6	28	A10	28
7	M2_Wn	7	29	A11	29
8	GND	8	30	A12	30
9	M2_TRISTn	9	31	A13	31
10	TRIGb	10	32	A14	32
11	VCC	11	33	A15	33
12	M1_Vp	12	34	A16	34
13	M1_Wp	13	35	VCC	35
14	M1_Vn	14	36	A17	36
15	M1_Wn	15	37	NC	---
16	A0	16	38	LED0	38
17	A1	17	39	DTEND1	39
18	A2	18	40	IIC_SCL	40
19	A3	19	41	IIC_SDA	41
20	A4	20	42	PIN42	42
21	VCC	21	43	DLCD4	43
22	A5	22	44	GND	44

Table 9-1: J1 microcontroller header

J2					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	DLCD5	45	23	IRQ2	67
2	DLCD6	46	24	IRQ3	68
3	DLCD7	47	25	TRIGa	69
4	VCC	48	26	PIN70	70
5	PIN49	49	27	NC	71
6	IRQ7_ADTRGn	50	28	WRHn	72
7	ASEMD0n	51	29	WRLn_WRn	73
8	RDn	52	30	VCC	74
9	WDT_OVFn	53	31	CS1n	75
10	A18	54	32	CS0n	76
11	A19	55	33	TCLKD	77
12	A20	56	34	TCLKC	78
13	GND	57	35	UD	79
14	A21	58	36	CS2n	80
15	A22	59	37	M1_Up	81
16	M1_TRISTn	60	38	M1_Un	82
17	PIN61	61	39	DACK1	83
18	PIN62	62	40	PIN84	84
19	IRQ0	63	41	DREQ1	85
20	GND	64	42	GND	86
21	IRQ1	65	43	PIN87	87
22	VCC	66	44	IO_7	88

Table 9-2: J2 microcontroller header

J3					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	IO_6	89	23	D5	111
2	IO_5	90	24	D4	112
3	IO_4	91	25	D3	113
4	IO_3	92	26	D2	114
5	IO_2	93	27	D1	115
6	VCC	94	28	D0	116
7	IO_1	95	29	GND	117
8	GND	96	30	CON_XTAL	118
9	IO_0	97	31	MD1	119
10	D15	98	32	CON_EXTAL	120
11	D14	99	33	MD0	121
12	D13	100	34	NMI	122
13	D12	101	35	FWE	123
14	VCC	102	36	PIN124	124
15	D11	103	37	PIN125	125
16	GND	104	38	DLCDE	126
17	D10	105	39	DLCDRS	127
18	D9	106	40	VCC	128
19	D8	107	41	NC	---
20	D7	108	42	NC	---
21	VCC	109	43	PIN131	131
22	D6	110	44	RESn	132

Table 9-3: J3 microcontroller header

J4					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	TIOC0A	133	23	PIN155	155
2	TIOC0B	134	24	AVSS	156
3	TIOC0C	135	25	AN6	157
4	VCC	136	26	AN7	158
5	TMR0	137	27	PIN159	159
6	RXD3	138	28	PIN160	160
7	TXD3	139	29	VREF	161
8	TMR1_SCK3	140	30	AVCC	162
9	GND	141	31	GND	163
10	AVSS	142	32	RXD0	164
11	ADPOT_AN0	143	33	TXD0	165
12	AN1	144	34	SCK0	166
13	AN8	145	35	PTRX	167
14	AN9	146	36	VCC	168
15	AN2	147	37	PTTX	169
16	AN3	148	38	SCK1	170
17	AN10	149	39	RXD2	171
18	AN11	150	40	TMS_SCK2	172
19	AVCC	151	41	NC	---
20	AN4	152	42	TRSTn_M2Up	174
21	AN5	153	43	TDI_TXD2	175
22	PIN154	154	44	TDO_M2Un	176

Table 9-4: J4 microcontroller header

9.2. Application Headers

Standard application header connections are detailed in this section.

* marks pins where a link to the microcontroller pin is via a fitted 0R link

JA1							
Pin	Header Name	CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	5V	CON_5V	---	14	DAC1	---	---
2	0V(5V)	GROUND	---	15	IO_0	IO_0	97
3	3V3	CON_3V3	---	16	IO_1	IO_1	95
4	0V(3V3)	GROUND	---	17	IO_2	IO_2	93
5	AVcc	CON_AVCC	151, 162	18	IO_3	IO_3	92
6	AVss	AVSS	142, 156	19	IO_4	IO_4	91
7	AVref	CON_VREF	161	20	IO_5	IO_5	90
8	ADTRG	IRQ7_ADTRGn	50	21	IO_6	IO_6	89
9	AD0	AN0	143*	22	IO_7	IO_7	88
10	AD1	AN1	144	23	IRQ3	IRQ3	68
11	AD2	AN2	147	24	IIC_EX	---	---
12	AD3	AN3	148	25	IIC_SDA	IIC_SDA	41
13	DAC0	---	---	26	IIC_SCL	IIC_SCL	40

Table 9-5: JA1 Standard Generic Header

JA2							
Pin	Header Name	CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	RESn	RESn	132	14	Un	M1_Un	82
2	EXTAL	CON_EXTAL	120	15	Vp	M1_Vp	12
3	NMIn	NMI	122	16	Vn	M1_Vn	14
4	Vss1	GROUND	-	17	Wp	M1_Wp	13
5	WDT_OVF	WDT_OVFn	53	18	Wn	M1_Wn	15
6	SCIaTX	TxD0	165	19	TMR0	TMR0	137
7	IRQ0	IRQ0	63	20	TMR1	TMR1	140
8	SCIaRX	RXD0	164	21	TRIGa	TRIGa	69
9	IRQ1	IRQ1n	65	22	TRIGb	TRIGb	10
10	SCIaCK	SCK0	166	23	IRQ2	IRQ2	67
11	UD	UD	79	24	TRISTn	M1_TRISTn	60
12	CTSRTS	---	---	25	Reserved		
13	Up	M1_Up	81	26	Reserved		

Table 9-6: JA2 Standard Generic Header

JA3							
Pin	Header Name	CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	Address Bus	A0	16	26	Read/Write Control	WRn	73*
2	Address Bus	A1	17	27	Memory Select	CS0n	76
3	Address Bus	A2	18	28	Memory Select	CS1n	75
4	Address Bus	A3	19	29	Data Bus	D8	107
5	Address Bus	A4	20	30	Data Bus	D9	106
6	Address Bus	A5	22	31	Data Bus	D10	105
7	Address Bus	A6	24	32	Data Bus	D11	103
8	Address Bus	A7	25	33	Data Bus	D12	101
9	Address Bus	A8	26	34	Data Bus	D13	100
10	Address Bus	A9	27	35	Data Bus	D14	99
11	Address Bus	A10	28	36	Data Bus	D15	98
12	Address Bus	A11	29	37	Address Bus	A16	34
13	Address Bus	A12	30	38	Address Bus	A17	36
14	Address Bus	A13	31	39	Address Bus	A18	54
15	Address Bus	A14	32	40	Address Bus	A19	55
16	Address Bus	A15	33	41	Address Bus	A20	56
17	Data Bus	D0	116	42	Address Bus	A21	58
18	Data Bus	D1	115	43	Address Bus	A22	59
19	Data Bus	D2	114	44	External Device Clock	---	---
20	Data Bus	D3	113	45	Memory Select	CS2n	80
21	Data Bus	D4	112	46	Bus Control	---	---
22	Data Bus	D5	110	47	Data Bus Strobe	WRHn	72
23	Data Bus	D6	108	48	Data Bus Strobe	WRLn	73
24	Data Bus	D7	107	49	Reserved	---	---
25	Read/Write Control	RDn	52	50	Reserved	---	---

Table 9-7: JA3 Standard Generic Header

JA5							
Pin	Header Name	CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	AD4	AN4	152	13	Reserved		
2	AD5	AN5	153	14	Reserved		
3	AD6	AN6	157	15	Reserved		
4	AD7	AN7	158	16	Reserved		
5	CAN1TX	---	---	17	Reserved		
6	CAN1RX	---	---	18	Reserved		
7	CAN2TX	---	---	19	Reserved		
8	CAN2TX	---	---	20	Reserved		
9	Reserved			21	Reserved		
10	Reserved			22	Reserved		
11	Reserved			23	Reserved		
12	Reserved			24	Reserved		

Table 9-8: JA5 Standard Generic Header

JA6							
Pin	Header Name	CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	DREQ	DREQ1	85	13	Reserved		
2	DACK	DACK1	83	14	Reserved		
3	TEND	DTEND1	39	15	Reserved		
4	STBYn	---	---	16	Reserved		
5	RS232TX	RS232TX	---	17	Reserved		
6	RS232RX	RS232RX	---	18	Reserved		
7	SCIbRX	RxD2	171	19	Reserved		
8	SCIbTX	TxD2	175*	20	Reserved		
9	SCIcTX	TxD3	139	21	Reserved		
10	SCIbCX	SCK2	172*	22	Reserved		
11	SCIcCK	SCK3	140*	23	Reserved		
12	SCIcRX	RxD3	138	24	Reserved		

Table 9-9: JA6 Standard Generic Header

Chapter 10.Code Development

10.1. Overview

Note: For all code debugging using Renesas software tools, the CPU board must either be connected to a PC serial port via a serial cable or a PC USB port via an E8. An E8 is supplied with the RSK product.

The HMON embedded monitor code is modified for each specific Renesas microcontroller. HMON enables the High-performance Embedded Workshop (HEW) development environment to establish a connection to the microcontroller and control code execution. Breakpoints may be set in memory to halt code execution at a specific point.

Unlike other embedded monitors, HMON is designed to be integrated with the user code. HMON is supplied as a library file and several configuration files. When debugging is no longer required, removing the monitor files and library from the code will leave the user's code operational.

The HMON embedded monitor code must be compiled with user software and downloaded to the CPU board, allowing the users' code to be debugged within HEW.

Due to the continuous process of improvements undertaken by Renesas the user is recommended to review the information provided on the Renesas website at www.renesas.com to check for the latest updates to the Compiler and Debugger manuals.

10.2. Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 256k code and data. To use the compiler with programs greater than this size you will need to purchase the full tools from your distributor.

Warning: The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

10.3.Mode Support

The HMON library is built to support Single Chip mode only for the SH7086 family.

10.4. Breakpoint Support

Limited breakpoints can be located in ROM code. However, code located in RAM may have unlimited breakpoints. To debug with less intrusion you need to purchase the E10A-USB on-chip debugger at additional cost.

10.5. Code located in RAM

Double clicking in the breakpoint column in the HEW code window sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them. (See the Tutorial Manual for more information on debugging with the HEW environment.)

10.6. HMON Components

HMON is built along with the user's code. Certain elements of the HMON code must remain at a fixed location in memory. The HMON components and their size and location in memory are detailed in Table 10-1: Memory Map for HMON Components

For more information, refer to the map file when building the code.

Section	Description	Start Location	Size (H'bytes)
RESET_VECTOR	HMON Reset Vector (Vector 0) Required for Start-up of HMON	H' 0000 0000	0x0004
SCI_VECTORS	HMON Serial Port Vectors (Vector 220, 221, 222,223)	H' 0000 0370	0x0010
PHMON	HMON Code	H' 0000 3000	0x21A2
CHMON	HMON Constant Data	H' 0000 51A4	0x0140
BHMON	HMON Un-initialised data	H' FFFF B900	0x0259
UGenU	FDT User Mode Micro Kernel This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 0000 1000	0x19C4
CUser_Vectors	Pointer used by HMON to point to the start of user code.	H'0000 0800	0x0004

Table 10-1: Memory Map for HMON Components

10.7. Memory Map

The memory map shown in this section visually describes the locations of program code sections related to HMON, the FDT kernels and the supporting code within the ROM/RAM memory areas of the microcontroller.

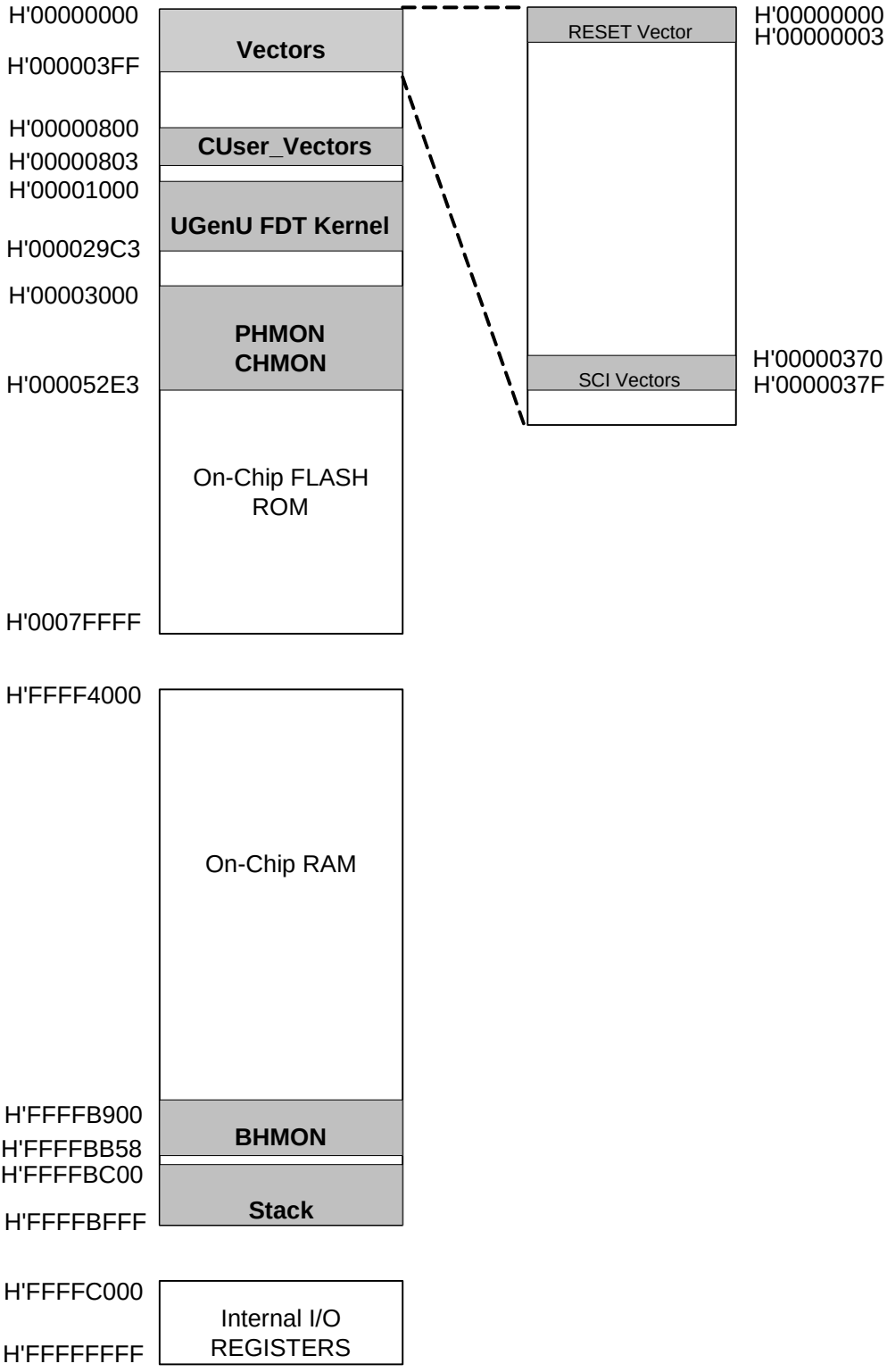


Figure 10-1: Memory Map

10.8. Baud Rate Setting

HMON is initially set to connect at 250000 Baud. The value set in the baud rate register for the microcontroller must be altered if the user wishes to change either the serial communication baud rate of the serial port or the operating frequency of the microcontroller. This value is defined in the hmonserialconfiguser.h file, as SCI_CFG_BRR (see the Serial Port section for baud rate register setting values). The project must be re-built and the resulting code downloaded to the microcontroller once the BRR value is changed. Please refer to the HMON User Manual for further information.

10.9. Interrupt mask sections

HMON has an interrupt priority of 15. Modules using interrupts should be set to lower than this value (14 or below), so that serial communications and debugging capability is maintained.

Chapter 11. Component Placement

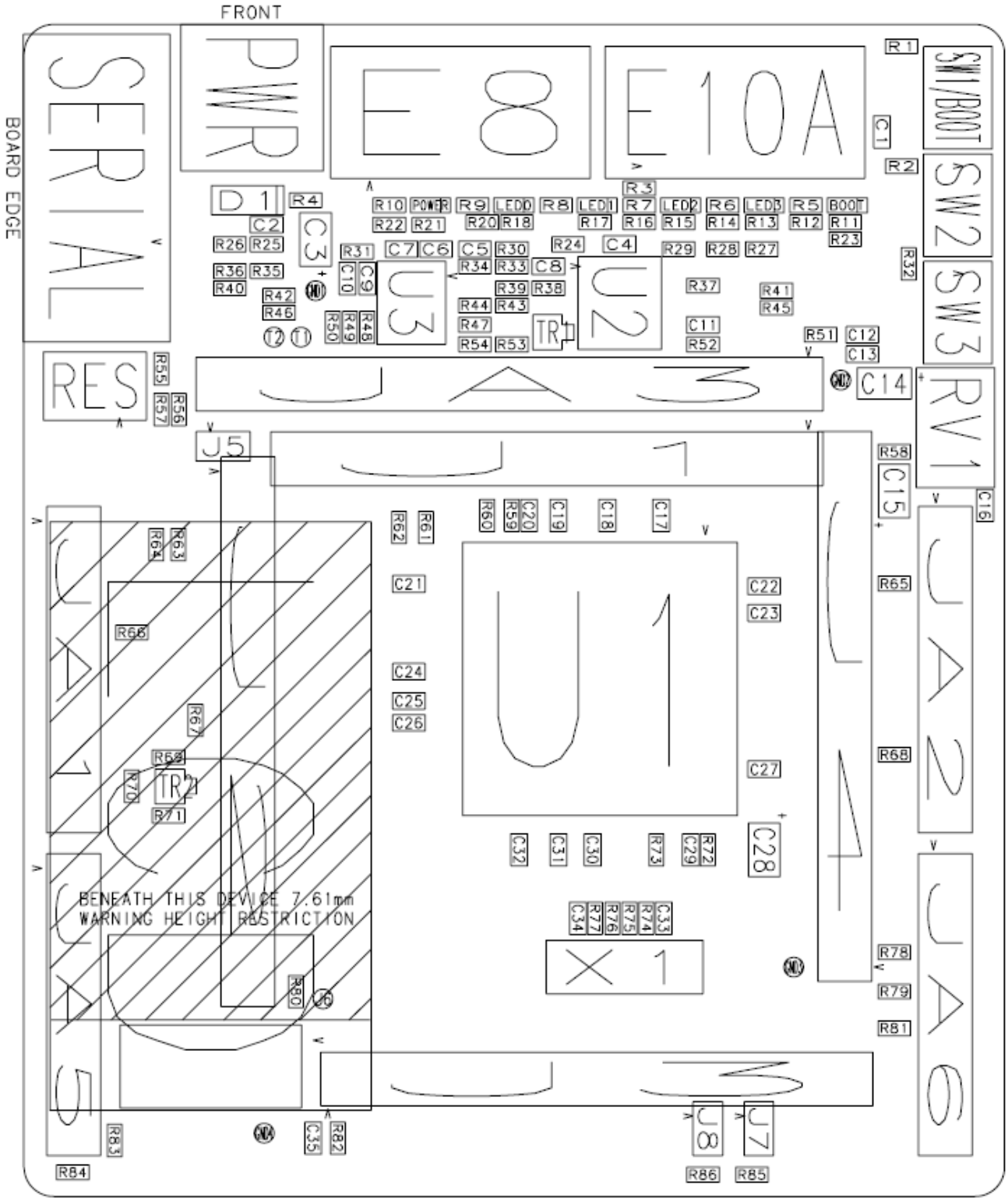


Figure 11-1: Component Placement (Top Layer)

Chapter 12. Additional Information

For details on how to use High-performance Embedded Workshop (HEW), refer to the HEW manual available on the CD or installed in the Manual Navigator.

For information about the SH7086 microcontrollers refer to the SH7080 Group *Hardware Manual*

For information about the SH7086 assembly language, refer to the SH-1/SH-2/SH-DSP *Software Manual*

Online technical support and information is available at: http://www.renesas.com/renesas_starter_kits

Technical Contact Details

America: techsupport.rta@renesas.com

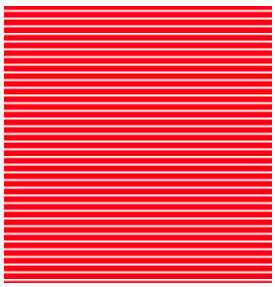
Europe: tools.support.eu@renesas.com

Japan: csc@renesas.com

General information on Renesas Microcontrollers can be found on the Renesas website at: http://www.renesas.com/

Renesas Starter Kit for SH7086
User's Manual
Publication Date Rev.1.00 13 March 2007
Published by: Renesas Technology Europe Ltd.
Duke’s Meadow, Millboard Road, Bourne End
Buckinghamshire SL8 5FH, United Kingdom

Renesas Starter Kit for SH7086
User's Manual



Renesas Technology Europe Ltd.
Dukes Meadow, Millboard Road, Bourne End Buckinghamshire SL8 5FH, United Kingdom